Amendments to the Claims

1. (Currently Amended): A computer-implemented method for designing circuits, comprising:

during a logical synthesis stage of a circuit design,

generating a network graph from a logical representation of the circuit design;

determining a structural metric from ~~a property of~~ the network graph, wherein the structural metric predicts congestion characteristics during optimization of the circuit design; and

using the structural metric during the logic synthesis stage to optimize the circuit design~~;~~.

2. (Previously Presented): The method of claim 1, wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises adding, deleting or substituting one or more circuits using a combination of boolean, algebraic and electrical optimizations.

3. (Previously Presented): The method of claim 1, wherein the structural metric includes a measure of routing congestion of the circuit design after placement and routing, the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design.

4. (Previously Presented): The method of claim 1, wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a technology independent synthesis stage of the logic synthesis stage.

5. (Previously Presented): The method of claim 1, wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a technology mapping stage of the logic synthesis stage.

6. (Previously Presented): The method of claim 1, wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a buffering stage of the logic synthesis stage.

7. (Previously Presented): The method of claim 1, further comprising incrementally updating the structural metric when logic changes are made to the circuit design.

8. (Previously Presented): The method of claim 7, wherein incrementally updating the structural metric when logic changes are made to the circuit design comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost.

9. (Previously Presented): The method as in claim 7, wherein incrementally updating the structural metric when logic changes are made to the circuit design comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary.

10. (Previously Presented): The method of claim 1, wherein the structural metric comprises any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric.

11. (Previously Presented): The method of claim 1, wherein determining a structural metric comprises:

generating one or more possible optimizations;

incrementally updating the structural metric when the optimizations are made to the circuit design to evaluate the cost of applying each of the one or more possible optimizations to the circuit design, the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric;

evaluating a structural metric cost of each of the one or more possible optimizations as given by the structural metric;

selecting an optimization from the one or more possible optimizations with the lowest structural metric cost; and

applying the optimization to the circuit design.

12. (Original): The method of claim 11, wherein generating the one or more possible optimizations comprises:

generating a structure-driven kernel factoring;

generating a structure-driven decomposition;

generating a structure-driven tech mapping; and

generating a structure-aware buffering.

13. (Currently Amended): A machine-readable medium having instructions stored thereon for optimizing a circuit design model during logic synthesis, comprising the steps of:

during a logical synthesis stage of a circuit design,

generating a network graph from a logical representation of the circuit design;

determining a structural metric from ~~a property of~~ the network graph, wherein the structural metric predicts congestion characteristics during optimization of the circuit design; and

using the structural metric during logic synthesis to optimize the circuit design.

14. (Currently Amended): A system for designing circuits, comprising:

means for creating a structural metric from ~~a property of~~ a network graph during a logical synthesis stage of a circuit design, wherein the network graph is derived from ~~a~~ logical representation of the circuit design, and the structural metric predicts congestion characteristics during optimization of the circuit design; and

means for using the structural metric during the logic synthesis stage to optimize the circuit design.